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PICO-SOM
System on Module

Pico SOM Card Model: pSOC-M10

Features

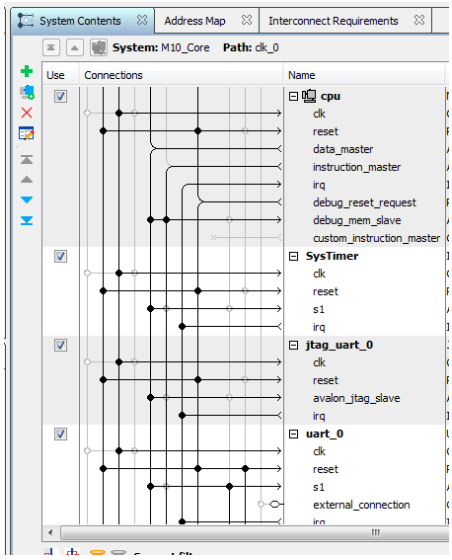
- Single 3V3 Power Supply
- MAX10 Fpga TQFP144 footprint can Host from 10M08 up to 10M50 Fpga, upto:
  - 50KLE
  - 1638 Kbytes Memory (Ram or Rom)
  - 746 Kbytes user Flash
  - 144 18 bits Multipliers
- Simply, easy to user, Two Dual Row 34 ways I/O connectors.
- 55 IO LVTTL User I/O
  - 5 shared with SPI
  - 6 can operate as ADC inputs with optional RC filters
  - 5 can operate as clock out
  - 3 can operate as clock inputs
- 1xRS232 input & 1xRS232 Output
- 1 SPIi with 2 Chips Select
- EEPROM, 32 Kbytes
- SRAM, 2Mbytes (1Mx16)
- 1 reset push button
- 1 Power monitor and Reset
- Fully-compatible with JTAG/IEEE 1149.1 boundary-scan standard
- Board Size 60x40x8mm

INTEL® MAX® 10 FPGAS

PRODUCT LINE	10M08	10M16	10M50
LEs (K)	8	16	50
Block memory (Kb)	378	549	1,638
User flash memory[1] (KB)	32 – 172	32 – 296	64 – 736
18 x 18 multipliers	24	45	144
Phase-locked loops (PLLs)[2]	1, 2	1, 4	1, 4
Internal configuration	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]	1, 1	1, 1	2, 1

Description

This GEB Pico-SOM is tailored build to menage the I/O and communication controller in the smart sub systems. It contains everything you need to start using the advanced features of Altera MAX10 family features. The baseboard version sockets a 10M08SAE144C8G device in a TQFP144 package, allowing hosting of others MAX10 devices up to 10M50SAE144C8G, the biggest one.



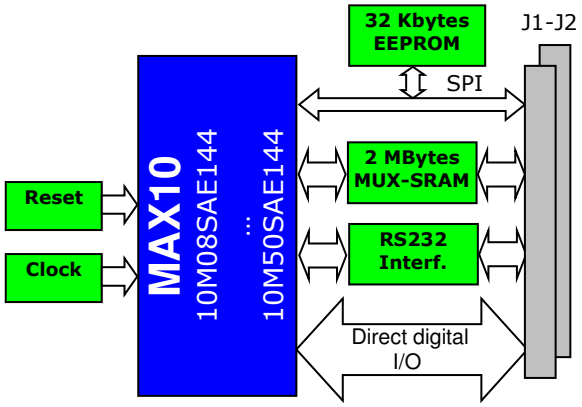
All technology Fpga requirements, power management, distribution and decoupling, fine pitch package connection, multilayer PCB manufacturing, double side PCB mounting and testing are met by Pico-SOM board. One TAP interface supports in-system programming (ISP) using Altera Byte Blaster. It allows also JTAG programming and testing.

The SocCard has on-board the resources to allow to efficient use of the FPGA, NIOS-II 32bits micro Controller softcore and all available IP, make simple the implementation of subsystems infrastructure (Power on reset, core power supply and decoupling, clock distribution, USB and/or RS232 and/or CAN interface). This providing benefits to the user that can focus only on its system.

Precompiled Board Support Package (BSP) and QSYS System Editors allows the user to easy fit on the Soc Boards customized version of Altera NIOS-II softcore. A large set of NIOS-II Peripherals or GEB peripherals IP can be connected to NIOS-II Avalon I/O bus to generate a specific application control system on SocCard.

The 2Mbytes SRAM extends NIOS-II capability allowing a data size handling that that would'nt be allowed by on chip ram only. The EEPROM device allows storing of setup parameter and/or events data logging.

Block Diagram & I/O connectors



J1			
Function	Pin Num.	Pin Num.	Function
+3V3	33	34	+3V3
IO0/ADCIN2	31	32	IO1/ADCIN3
TDO	29	30	TMS
TCK	27	28	TDI
CONFIG#	25	26	PFAIL
I_CKI3	23	24	IO2
IO3/ADCIN4	21	22	IO4/ADCIN5
IO6/ADCIN7	19	20	IO5/ADCIN8
IO7	17	18	IO_CKO1
IO_CKO0	15	16	IO8
IO9	13	14	IO10
IO11	11	12	IO12
IO13	9	10	IO14
IO15	7	8	IO16
IO17	5	6	IO18
IO19	3	4	IO20
GND	1	2	GND

J2			
Function	Pin Num.	Pin Num.	Function
TXD1	33	34	RXD1
IO40	31	32	IO45/POR_n
IO39	29	30	IO44/SSCLK
IO_CKO2	27	28	SPI-SDI
IO38	25	26	IO43/SPI-DO
IO37	23	24	IO42/SPI-CSV
IO36	21	22	IO41/SPI-CSI
I_CKI4	19	20	IO35
I_CKI6	17	18	IO_CKI5
IO34	15	16	IO_CKI7
IO41	13	14	IO33
IO31	11	12	IO32
IO29	9	10	IO30
IO27	7	8	IO28
IO25	5	6	IO26
IO23	3	4	IO24
IO21	1	2	IO22

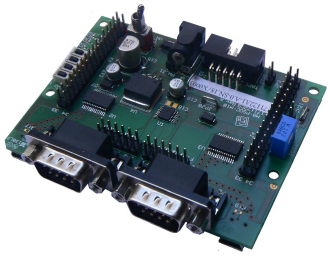
The pSOC-M10 hosts 2Mbytes of SRAM, one RS232 interface, one SPI interface with 3 chip select of which one is used to enable the 32Kbytes EEPROM. The two SMT header connettor, 32 ways, make easy the installation on simple cards 2-4 layers "carrier" thus allowing a quick assessment of the potential of the Soc card itself.

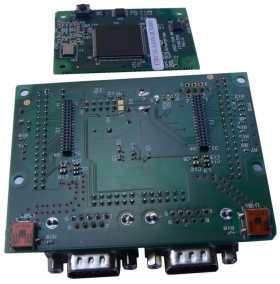
Applications

Typical applications of this SOM are in the "Smart Core" of smal smart subsystem such as Motors, sensors position, graphic leds matrix, communication controller in digital, analog and power signals, management of setup parameters, command, status and faults. In the typical application, the SOM module is hosted on an application board such as a doughter. The application board must host the application interfaces circuities and the physical interfaces of the SOM communication channel, such as RS4222/RS485, USB, CAN and so on.

Starter Kit

The starter kit includes a carrier board and a HW/SW NIOS-II system.





The carrier board adds some I/O resources using some pSOC I/O pins, it also carries out the others I/O by 2x34ways 2.54mm pitch headers. The added resources are: 2xUSB ports, 2XRS232 Ports, DC power supply connectors, 4 push buttons, 4 leds. One trimmer can generates an analog input to ADC allowing tests of ADC related HW o SW. A 2.54mm 10 ways header connector carries out the TAP signals, allowing the ISP and the debug.

The HW/SW NIOS-II system includes one QSYS system able to interface the SUB/UARTS port, the ADC, the Multiplexed SRAM, the I/O headers by PIO. The software allows access to ports and an example of interrupt handling.

Ordering Information

GEB Code	Description
171017A1	FPGA 10M08SAE144C8, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, without filters on ADC inputs
171017A2	FPGA 10M08SAE144C8G, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, with filters on ADC inputs
171017A3	FPGA 10M50SAE144C8G, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, without filters on ADC inputs
180199K1	Starter KIT, 1x171017A1 pSoc-M10 Card, 1x171122A1 pSoc Carrier, NIOS-II HW/SW QSYS system

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