GEB Enterprise S.r.l.
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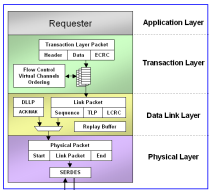
VHDL and ALTERA QUARTUS II Courses

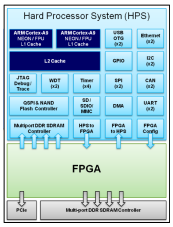
La **GEB Enterprise S.r.l.** is an **ATPP** (Altera Technical Training Partner) and **DSN** (Design Service Network) certified partner of Altera, a leading company in FPGA market, and AAP certified partner of JTAG Technologies, organizes courses VHDL for FPGA VHDL design, for System On Programmable Chip (SOPC), for BSCAN DFT (Design For Test , BSCAN oriented), for JTAG test operators. The courses range from the VHDL language, with source level simulation in a vendor independent platform (Aldec Active HDL and/or ModelSim) to the coding-oriented synthesis. The methodologies of synthesis and optimization are focused on Altera Quartus II platform.

VEC222-Creating PCI Express Links Using FPGAs



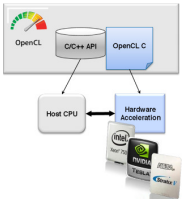
The course will start with a high-level overview of the PCI Express protocol and from there you'll learn the design flow to target the Hard IP for PCI Express blocks found in Cyclone® V, Arria® V and Stratix® V devices, particularly when using the Qsys system design tool. You'll see how to debug and test your PCIe links, both through simulation and in-system. You'll discover advanced device features to add more flexibility and capability to your PCI Express-based design. By the end of the training, you'll feel comfortable getting your own device's PCIe link up and running.

VEC221 Designing with an ARM-based SoC



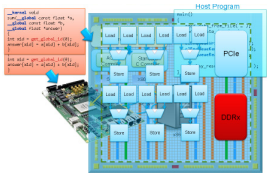
This course is intended for hardware and firmware engineers and will leverage your knowledge of Qsys system design to guide you on implementing an Altera® SoC with the ARM® Cortex A9 hard processing system (HPS). This course focuses on the hardware aspects of using the processor in the SoC from the design, verification and debug hardware perspectives just as if the processor was external. Our intention is that you feel completely comfortable using the HPS in the SoC and know all of the resources at your disposal to work with the board designer, FPGA engineer, firmware engineer or software engineer to get up and running quickly.

VEC311- Parallel Computing with OpenCL



OpenCL is a standard for writing parallel programs for heterogeneous systems. In the FPGA environment, OpenCL constructs are synthesized into custom logic. This course introduces the basic concepts of parallel computing. It covers the constructs of the OpenCL standard & Altera flow that automatically converts kernel C code into hardware that interacts with the host. In hands-on labs, you'lll write programs to run on both the CPU & FPGA. Note. This hands-on workshop provides an introduction to OpenCL for FPGAs. For in-depth training on OpenCL & Altera's OpenCL for FPGAs solution attend the "OpenCL for Altera FPGAs" class from an ATPP partner.

VEC321- Optimizing OpenCL for Altera FPGAs

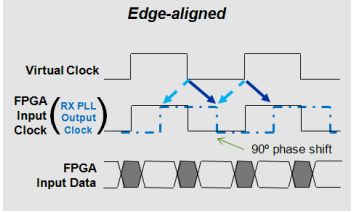


This course covers the optimization techniques needed to implement a high performance OpenCL solution on an FPGA using the Altera SDK for OpenCL. We will discuss good coding design practices, ways to improve data processing efficiency, memory access efficiencies, and host side optimizations. We will also focus on Altera SDK for OpenCL specific features that can significantly improve OpenCL performance on FPGAs compared to other platforms.

VEC107-QUARTUS II: Introduction to Timing Analysis

You will learn how to constrain & analyze a design for timing using the **TimeQuest** timing analyzer in the Quartus® II software. This includes understanding FPGA timing parameters, writing Synopsys Design Constraint (SDC) files, generating various timing reports in the TimeQuest timing analyzer & applying this knowledge to an FPGA design. Besides learning the basic requirements to ensure that your design meets timing, you will see how the TimeQuest timing analyzer makes it easy to create timing constraints to help you meet those requirements.

VEC125-QUARTUS II: Advanced Timing Analysis with TimeQuest



Using the Quartus® II software and building upon your basic understanding of creating Synopsys Design Constraint (SDC) timing constraints, this class will guide you towards understanding, in more depth, timing exceptions. You will learn how to apply timing constraints to more advanced interfaces such as source synchronous single-data rate (SDR), double-data rate (DDR) and LVDS, as well as clock and data feedback systems. You will discover how to write timing constraints directly into an SDC file rather than using the GUI and then enhance the constraint file using TCL constructs. You will also perform timing analysis through the use of TCL scripts.

VEC110- System Integration with Qsys This class will teach you how to quickly build designs for Altera FPGAs using Altera's Qsys system-level integration tool. You will become proficient with Qsys and will expand your knowledge of the Quartus® II FPGA design software. You will learn how to build hierarchical systems, how to quickly integrate IP and custom logic into a system, and also how to optimize designs for performance. Since Qsys makes design reuse easy through standard interfaces, we will dive deeply into the Avalon-Memory Mapped and Streaming Interfaces. The class provides a significant hands-on component, where you will gain significant exposure to tool usage as well as system and custom HDL component design

VEC220- Designing with DSP Builder Advanced Blockset Learn the timing-driven Simulink® design flow to implement high-speed DSP designs. This course focuses on implementing DSP algorithms using the advanced blockset capability of DSP Builder—an interface between Quartus® II software & MATLAB® and Simulink from MathWorks. You'll analyze & design your DSP algorithm using the DSP Builder advanced blockset in MATLAB & Simulink. You'll explore architecture & performance tradeoffs with system-level constraints. Also you'll verify functionality & performance of generated hardware in the Quartus II software. Finally, you'll speed design time by incorporating ready made ModelIP cores in your design.

VEC100-Introduction to VHDL This two-day course is a general introduction to the VHDL language and its use in programmable logic design. The emphasis is on the synthesis constructs of VHDL; however, you will also learn about the simulation constructs. You will gain a basic understanding of VHDL to enable you to begin creating your design file. In the hands-on laboratory sessions, you will put this knowledge to the test by writing simple but practical designs. You will also learn the basic instructions needed for operating both the synthesis and simulation tools of the QuartusII.

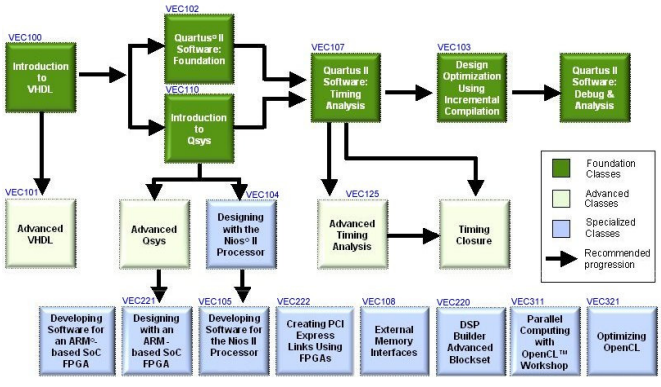
VEC101-Advanced VHDL Design Techniques In this course, you will learn & practice efficient coding techniques for VHDL synthesis. You will gain experience writing behavioral & structural code & learn to effectively code common logic functions including registers, memory & arithmetic functions. You will use VHDL constructs to parameterize your designs to increase their flexibility and reusability. While the concepts presented will mainly be targeting Altera® devices using the Quartus® II software environment, many can be applied to synthesizing hardware using other synthesis tools as well. You will also be introduced to testbenches, VHDL constructs used to build them & common ways to write them. The hands-on exercises will use Quartus II software to process VHDL code and ModelSim®-Altera software for simulation.

VEC102-QUARTUS II: Foundation You will learn how to use the Quartus® II software to develop an FPGA or CPLD. You will create a new project, enter in new or existing design files, and compile your design. You will also learn about timing constraints and analyze a design compiled with these constraints using the TimeQuest timing analyzer, the path-based static timing analysis tool included with the Quartus II software. You will learn techniques to help you plan your design. You will employ QuartusII features that can help you achieve design goals faster. You will also learn how to plan and manage I/O assignments for your target device.

VEC104-NIOS II and QSYS This course will teach you how to design in a soft core embedded processor with an Altera FPGA. This course is focused on the hands-on development of Nios II hardware using the Nios II Development Kit. You will learn how to integrate a Nios II 32-bit microprocessor and test it in an Altera FPGA. You will learn how to configure and compile designs using the Quartus II software and QSYS. You will participate in discussions about the features and capabilities of the development board along with how to create and test your own custom IP or custom Instruction. The training is hardware designer oriented with some hint on HAL driver design and software design in the Eclipse environment. After taking this course you should feel confident tackling your next SOPC design

Courses Organization

GEB organizes training courses that make the attendees able to design systems on programmable chip (SOPC) with a 32 Bits multiprocessor architectures, 32Bit NiosII embedded CPU, integrated into the Altera **QSYS**, with peripherals and custom instructions to increase system performance. The courses can take place in specific GEB partner's classrooms or at the Customer premises. All courses are confirmed when a minimum of n°4 attendees is achieved. More sessions are organized for a number of attendees exceeding n°10. Attendees will receive electronic and/or printed versions of the course materials: photocopies of slides, practical examples, CD with the exercises. At the end of the course a certificate of participation is issued



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